A High-Temperature SiC Three-Phase AC–DC Converter Design for >100 °C Ambient Temperature

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Abstract—**High-temperature (HT) converters have gained importance in industrial applications where the converters operate in a harsh environment, such as in hybrid electrical vehicles, aviation, and deep-earth petroleum exploration. These environments require the converter to have not only HT semiconductor devices (made of SiC or GaN), but also reliable HT packaging, HT gate drives, and HT control electronics. This paper describes a detailed design process for an HT SiC three-phase PWM rectifier that can operate at ambient temperatures above 100 °C. SiC HT planar structure packaging is designed for the main semiconductor devices, and an edge-triggered HT gate drive is also proposed to drive the designed power module. The system is designed to make use of available HT components, including the passive components, silicon-on-insulator chips, and auxiliary components. Finally, a 1.4 kW lab prototype is tested in a harsh environment for verification.**

Index Terms—**Harsh environment, high-temperature (HT) converter, silicon carbide JFET, silicon-on-insulator (SOI) technology.**

I. INTRODUCTION

HIGH-TEMPERATURE (HT) converters have become more and more important in industrial applications where the converter operates in a harsh environment, such as hybrid electrical vehicles, aviation, and deep-earth petroleum exploration [1]–[3]. Compared to traditional silicon (Si) devices, new wideband gap devices, made of materials such as silicon carbide (SiC) or gallium nitride (GaN), provide much higher bandgap, thermal conductivity, and breakdown fields, which offers them the potential capability to overcome the temperature, frequency,

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and power management limitations of Si devices. Several publications have shown that SiC devices are capable of decreasing loss and increasing the device junction temperature, which will result in higher efficiency, a lighter cooling system, and higher power density [4]–[6]. In order to use this SiC HT characteristic, some publications have described HT packaging with SiC semiconductors [7]–[10]. However, these works still use the commercial technology that has been designed for Si devices, which may limit the advantages SiC semiconductors have in terms of faster switching speed. To fully utilize the SiC device's HT tolerance and fast-switching capability, a reliable HT packaging method is desired that will allow the SiC devices to achieve smaller parasitic.

Meanwhile, the harsh environment of some applications requires not only an HT semiconductor power module, but also HT gate drive circuits, HT control electronics, HT passive components and the like that are able to operate in these environments. These subfunctions of the converter need to be reliably designed with the limited selection of HT components that are available.

This paper presents the design process of an HT SiC three-phase ac/dc converter that can operate in ambient temperatures above 100 °C, and an SiC power module that can work with a 250 °C junction temperature. Taking into consideration the material available, SiC diodes and JFETs are used as the main circuit devices and are packaged in a novel HT planar structure. Besides the HT SiC power module, an HT transformer-isolated gate drive circuit is also proposed. Other functions such as the harmonic filter and the control system, including protection and sensor functions, are designed according to the available HT silicon-on-insulator (SOI) ICs and HT passive components.

Because of both the simple topology and the simple control, a typical single-switch three-phase boost PFC circuit [11] is used to demonstrate the concept of HT converter design. The structure and topology for the three-phase ac/dc rectifier are shown in Fig. 1. The power module is composed of seven SiC diodes and one normally ON SiC JFET. The first six diodes are utilized as a diode rectifier stage, and another diode and JFET make up the second boost stage. The input voltage is lower than 100 V (rms/phase), and the output voltage is regulated to 270 V. The system's power rating is 1.4 kW.

This paper is organized as follows. Section I provides the general topology of the proposed system and an introduction to the motivation behind this study. Section II describes the HT planar structure packaging for the multiple-chip power module. Section III presents the surveyed HT components besides the power module. Section IV shows the detailed HT system design
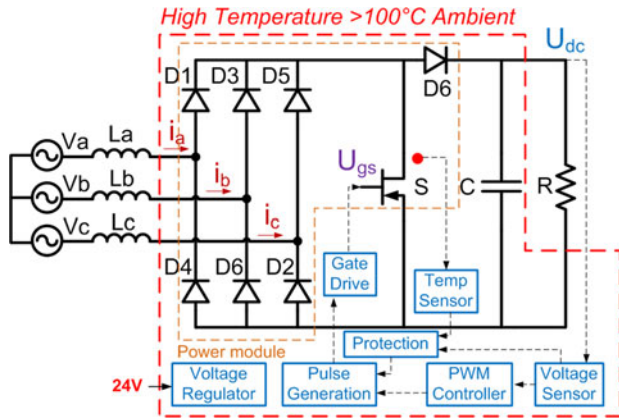
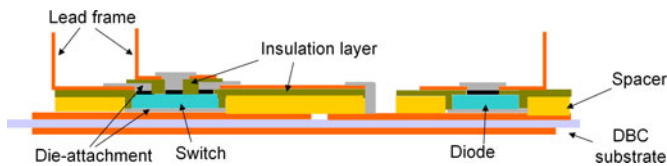Fig. 1.   System topology and configuration.

Fig. 2.   Package structure power module.

process. Section V gives the HT converter experimental results. Section VI provides the discussion based on the test results and, finally, Section VII provides the conclusions drawn from this paper.

II. SiC JFET PLANAR STRUCTURE PACKAGING

Traditionally speaking, the packaging structure can be divided into a wire-bonding structure and a planar structure. The wire-bonding packaging is widely utilized in industrial applications for its simplicity. On the other hand, in a planar structure, both the device's top and bottom pads are connected to the external lead frame without wires. Compared with the wire-bonding method, the planar packaging structure has several advantages, such as smaller footprint, smaller parasitic parameters, more flexible routing, and double-side cooling capability [12]–[14], which are very suitable for HT applications. With these considerations, this paper designs the HT SiC power module using the planar packaging method.

A cross-sectional diagram of the proposed planar structure power module is shown in Fig. 2. The bottom drain pad and cathode pad of the device and the diode are attached to the direct bond copper (DBC) with die-attachment material. Separated by the spacer and the insulation layer, the source and anode lead frames are attached above the substrate with windows in the middle for the topside soldering. The gate lead frame of the JFET is attached above the source frame, separated by another insulation layer and connected to the gate pad with another soldering process. No bonding wires are utilized to provide die attachment for this planar structure, unlike the wire-bonding structure. Meanwhile, since the lead frames are 3-D, more flexible routing and a smaller footprint are possible. However, in

order to fully utilize the HT characteristics of the SiC devices, HT materials need to be selected to build an HT planar structure power module.

SiC diodes and normally ON SiC JFETs from SiCed are selected for the power devices because of the state of material availability when the system was being designed.

The candidate materials for DBC substrates are listed in Table I. Compared with alumina (Al_2O_3), aluminum nitride (AlN) and silicon nitride (Si_3N_4) have smaller coefficients of thermal expansion (CTE), which can match better with SiC devices (CTE = 3). Because it has the highest thermal conductivity, easy processing, and lower cost, the AlN is selected. However, for high-current applications that need to employ more copper thickness, Si_3N_4 would be a good candidate because of its high flexural strength, which will increase the thermal reliability of the DBC.

Solder, silver glass, and nanosilver paste are summarized in Table II as candidates for the HT die-attachment material. Ag glass may crack during the processing, which will reduce the reliability of the component [16]. After comparison with HT solder, the nanosilver paste [17] is selected for the die-attachment material for two reasons. First, the fixed processing temperature of nanosilver paste (275 °C) will lead to a much lower processing temperature than the HT solder in the multiple-step die-attaching process that occurs in a planar structure power module. Second, because the device top pads are much smaller, as shown in Fig. 3, the nanosilver paste will keep its shape during the sintering process, which makes it easier to form the connection on the top of the device and provide more accurate alignment, which is very important in the planar structure power module.

Other materials selected for the prototype module are summarized in Table III. All of the materials are suitable for operation at 250 °C.

The fabrication process of the SiC power module is illustrated in Fig. 4. The patterned HT polyimide Kapton tape is attached to the DBC as both insulation and a spacer layer. Then, the device is positioned with the assistance of the spacers, and later attached to the DBC by sintering with nanosilver paste. In order to prevent electrical breakdown around the edges of the device, polyimide insulation material Epo-tek 600 is utilized to cover the device's guard rings and fill the gaps between the spacer and the device. Then, the source lead frame of the JFETs and the anode lead frame of the diode are bonded to the spacer by curing Epo-tek 600 in between the layers. In the next step, another sintering process is utilized to provide the connection of the source and anode pad to the lead frames. The second insulation layer is also formed by Epo-tek 600 on top of the source lead frame, and the gate lead-frame layer is bonded by curing the polyimide again. Afterward, the third sintering process connects the JFETs gate pad to the lead frames. Finally, adhesive epoxy Duralco 132 provides the connection between the power module and the heatsink. In total, the planar structure packaging has three sintering and two curing steps. Fig. 5 shows the prototype SiC power module in the planar structure. The static characterizations of the device show no visible changes before and after the packaging.

TABLE I
CANDIDATE MATERIALS FOR DBC SUBSTRATE [15]

Substrate	CTE (ppm/K)	Thermal Conductivity (W/m/K)	Dielectric Strength (kV/mm)	Tensile Strength (MPa)	Flexural Strength (MPa)
Al_2O_3	6.0	24	12	127.4	317
AlN	4.6	150-180	15	310	360
Si_3N_4	3.0	70	10	96	932

TABLE II
CANDIDATE MATERIALS FOR DIE ATTACHMENT

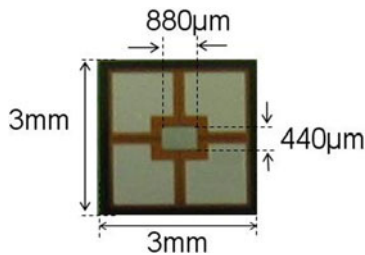| Different Materials	Processing temp (°C)	Working temp (°C)	Thermal Conductivity (W/m/K)	CTE (ppm/K)	Electrical resistivity ($10^{-6}\,\Omega\cdot$cm)
95% Pb- 5%Sn	350	310	32	28	20
80%Au- 20%Sn	320	280	57	16	17
80% Au- 20%Ge	390	360	88	13	30
Hysol Ag glass	400	900	40	16	54
Sintered Nano Ag	275	900	240	19	63

Fig. 3.   Pads of SiC JFET (1200 V, 5 A).

TABLE III
MATERIAL SELECTION SUMMARY FOR THE PLANAR STRUCTURE POWER MODULE

SiC JFET	1200V,5A 3mm×3mm from SiCed
SiC Diode	1200V,5A 2.7mm×2.7mm from SiCed
Substrate	AlN DBC (25 mils AlN, 8mils Cu)
Adhesive Epoxy	Duralco 132
Die-attachment	Nano-silver paste
Spacer	Kapton tape (2 mil)
Insulation layer	Epo-tek 600

Fig. 6 shows the fabricated power module forward characteristics test results with different junction temperatures. The fabricated power module is heated by a hot plate and the junction temperature is measured by the embedded T-type thermocouple. Both diode and JFET forward characteristics are recorded with respect to three different junction temperatures. Fig. 6(a) shows one of the SiC diode (D6) forward characteristics. By increasing the junction temperature, the on-resistance increases visibly

due to the reduction in the electron mobility at elevated temperatures. Fig. 6(b) illustrates the measured forward characteristics of the SiC JFET. The gate-to-source voltage was controlled as $0, -15, -20$, and -25 V. The threshold voltage of the SiC JFET is -22 V. Thus, -25 V gate-to-source voltage will guarantee turn-off of the JFET. Based on the test results, R_{dson} increases about threefold as the ambient temperature rises from 25 °C to 250 °C.

As mentioned previously, the planar structure utilizes a 3-D lead frame and provides a direct connection to the top side of the device without bonding wire, which will lead to smaller footprint and less parasitics. To demonstrate the advantages of the planar structure, both parasitic and electrical analysis needs to be conducted [18]. Ansoft Q3D software is first used as the simulation tool to analyze the parasitic between the wire bonding structure and the planar structure in the multiple-chip power module. Fig. 7(a) shows the system schematic with lumped parasitics. Fig. 7(b) and (c) shows two different packaging structures. Lead frames A, B, and C indicate the ac input terminal. P, N and G, S represent the dc output and gate control terminals.

The key parasitic [19], the gate loop inductance ($L_G + L_S$), the main loop inductance ($L_P + L_N + L_D + L_S$), and the common source inductance (L_S) are shown in Fig. 8. The planar structure power module shows a size reduction of almost 50%. Because of the reduced size and footprint, the main loop inductance of the planar structure power module is much smaller than the traditional wire bonding structure. Meanwhile, the lack of bonding wires in the gate loop for the planar structure will reduce both the gate loop impedance and reduce the coupling between the gate loop and the main loop that contributes to the common mutual loop inductance. The reduced parasitic will influence the performance for the power module.

Both the turn-on and the turn-off switching waveforms and the switching energy for planar structure and wire bonding structure are simulated and shown in Fig. 9 using the relevant parasitic
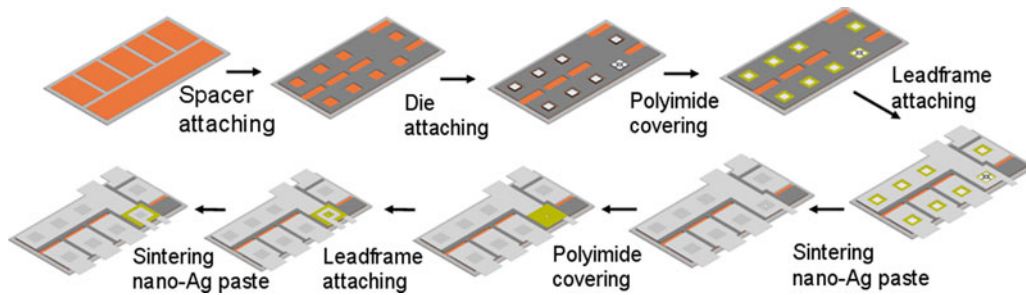
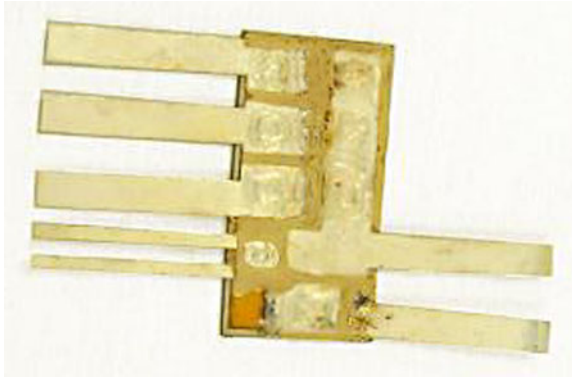Fig. 4.   Fabrication process.

Fig. 5.   Fabricated power module.

shown in Fig. 8. From the simulation results, we can see that the switching waveforms are less sensitive to the gate loop inductance than they are to the other two loops because there is more damping in the gate loop in forms such as gate resistance, JFET internal gate resistance, etc. However, the influence of the main loop and mutual loop inductance on the performance can be clearly seen from the simulation result. The planar structure reduces the main loop inductance from 26 nH with the wire bonding structure to 12 nH, which will reduce the JFET drain–source voltage spike from 295.7 to 279 V. The reduced mutual loop inductance in the planar structure will help to increase both the turn-on and turn-off current speed compared with the wire bonding structure. This can be explained by the negative feedback effect from the main loop to the gate loop. The voltage drop across the mutual inductance counteracts the change of gate voltage during the drain current change, which will slow it down [20]. Because of its reduced voltage spike and increased current speed, compared with the wire bonding structure, the hybrid structure will decrease the turn-on switch energy from 32.18 to 25.74 μJ and the turn-off switch energy from 68.7 to 54.1 μJ.

III. OTHER HT COMPONENTS

As shown in Fig. 1, in addition to the main circuit devices, the dc-link capacitor, voltage and temperature sensor, protection, pulsewidth modulation (PWM) controller, and gate drive circuits must also be able to operate in an HT environment.

For control electronics, the junction leakage current at HTs is a major concern in bulk CMOS processes, and can lead to the failure of the circuit in an HT environment. SiC-based devices are expected to be able to operate at up to 600 °C. However, there is no SiC-based integrated circuit manufacturing available yet. With the SOI technology, the leakage current for HT operation can be effectively reduced. As shown in Fig. 10, a buried insulator layer in the SOI structure greatly decreases the leakage path associated with the drain and the source p-n junction diodes. In addition, the threshold voltage variation with temperature is smaller in SOI devices than in bulk devices. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at higher temperatures. These properties make SOI-based circuits capable of operating successfully in the 200–300 °C temperature range, which is well above the range of conventional bulk silicon-based devices [21].

The HT resistors are surveyed and listed in Table V in the Appendix. HT thick-film resistors are selected during the design. The capacitors, which are rated for use at more than 200 °C, are surveyed and summarized in Fig. 12 and Table VI. The data come from both the manufacturers' websites and a literature survey. Generally speaking, three types of capacitors provide HT capability: ceramic, tantalum, and mica. As shown in Fig. 12, the tantalum capacitor covers a high-capacitance range with a very low voltage rating. Conversely, the mica capacitor covers a low-capacitance range with a high voltage rating. However, the ceramic capacitor fills the gap between the tantalum capacitor and mica capacitor. In our design, both the control and dc-link capacitors are ceramic capacitors. The HT magnetic components rated above 200 °C are summarized in Fig. 13 and Table VII. For applications requiring low-saturation flux and high operation frequency, most publications utilize ferrite magnetic core [22]–[25]. For high-saturation applications, such as a boost filter or an electromagnetic interference (EMI) filter in a high-power device, a nanocrystalline soft magnetic core could be a good candidate [26]. HT low-permeability NiZn ferrite toroid cores (4C65) from Ferroxcube are used in the gate drive transformer design.

We chose to use 95% Pb–5% Sn HT solder from Amerway to solder the motherboard components. Advanced Circuits provides the HT hydrocarbon ceramic material laminate printed circuit board (PCB) (Rogers 4350), which can operate at temperatures up to 280 °C, and be utilized to build the motherboard.
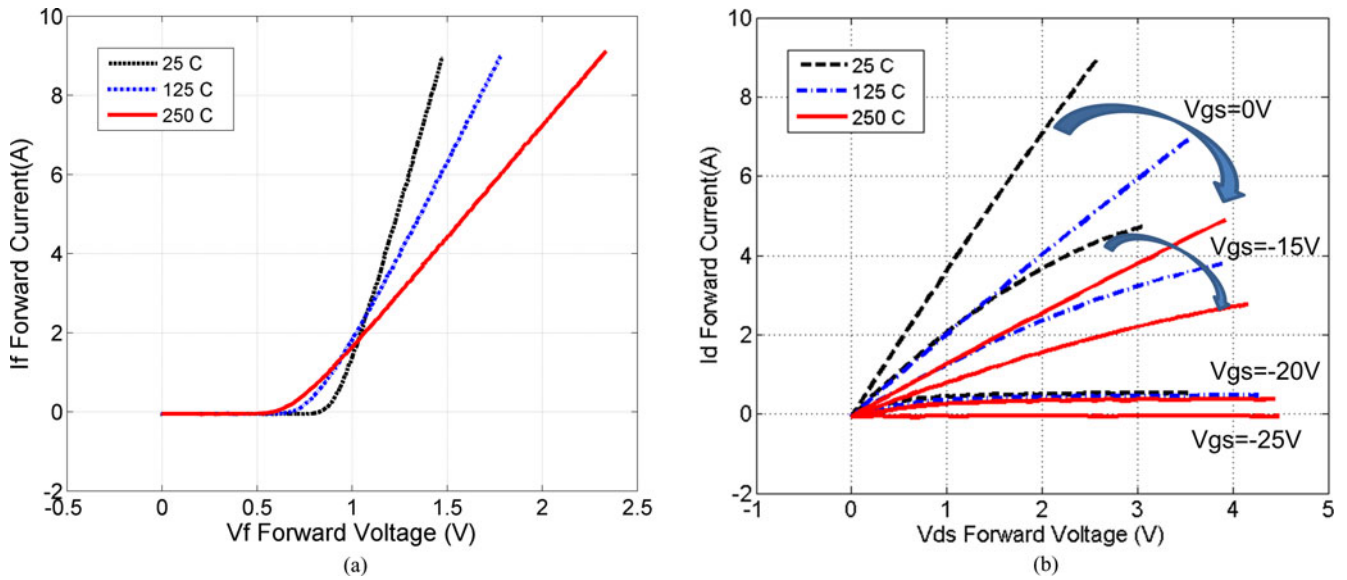
Fig. 6. Fabricated power module forward characteristics test. (a) Diode (*D*6) forward characteristics. (b) JFET (S) forward characteristics.
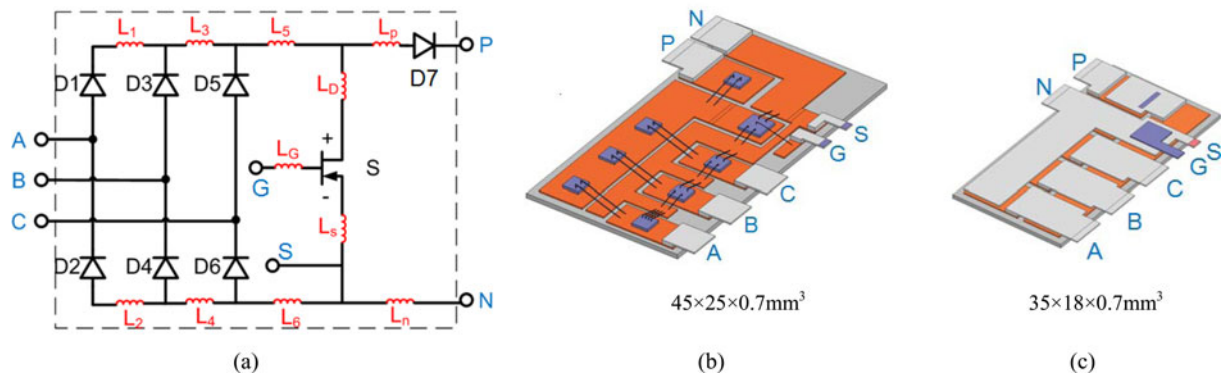

Fig. 7. Parasitic comparison between wire bonding structure and planar structure. (a) System schematic. (b) Wire bonding structure. (c) Planar structure.
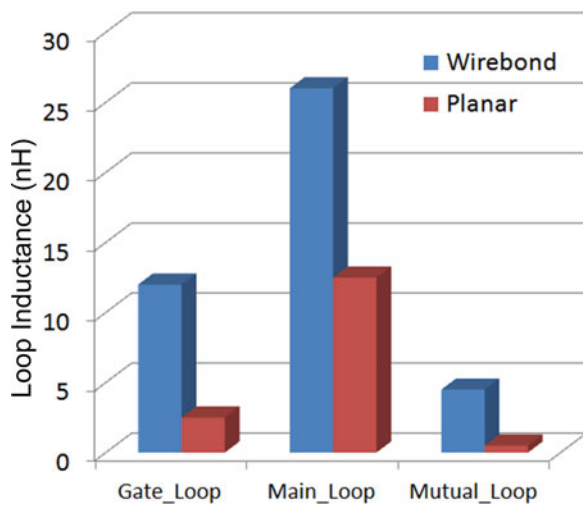

Fig. 8. Parasitic comparison results.

The thermal reliability characteristics of some of the selected components are also tested in the converter design, and the results are shown in the following sections.

IV. HT THREE-PHASE RECTIFIER SYSTEM DESIGN

A. System Structures and Functions

Fig. 14 shows the system structure and motherboard functions for the three-phase PWM rectifier. In addition to the power module and heatsink, an HT motherboard is designed to be placed on top of the power module. HT ceramic dc-link capacitors are put on top of the motherboard to filter high-frequency current, and a voltage sensor circuit and a temperature sensor circuit are implemented to sense the dc-link voltage and the device junction temperature. Using these sensors and protection circuits, the protection mode will be activated if the voltage and temperature are higher than the threshold values. Other functions implemented in the motherboard are the PWM controller, voltage regulator, pulse generation, and gate drive circuit.

Cissoid and Honeywell are two major suppliers that provide HT SOI semiconductor solutions. The typical SOI components include voltage regulators, voltage references, clock generators and timers, analog-to-digital converters, amplifiers, power MOSFETs, and drivers. Some of the SOI components are shown in Fig. 11.
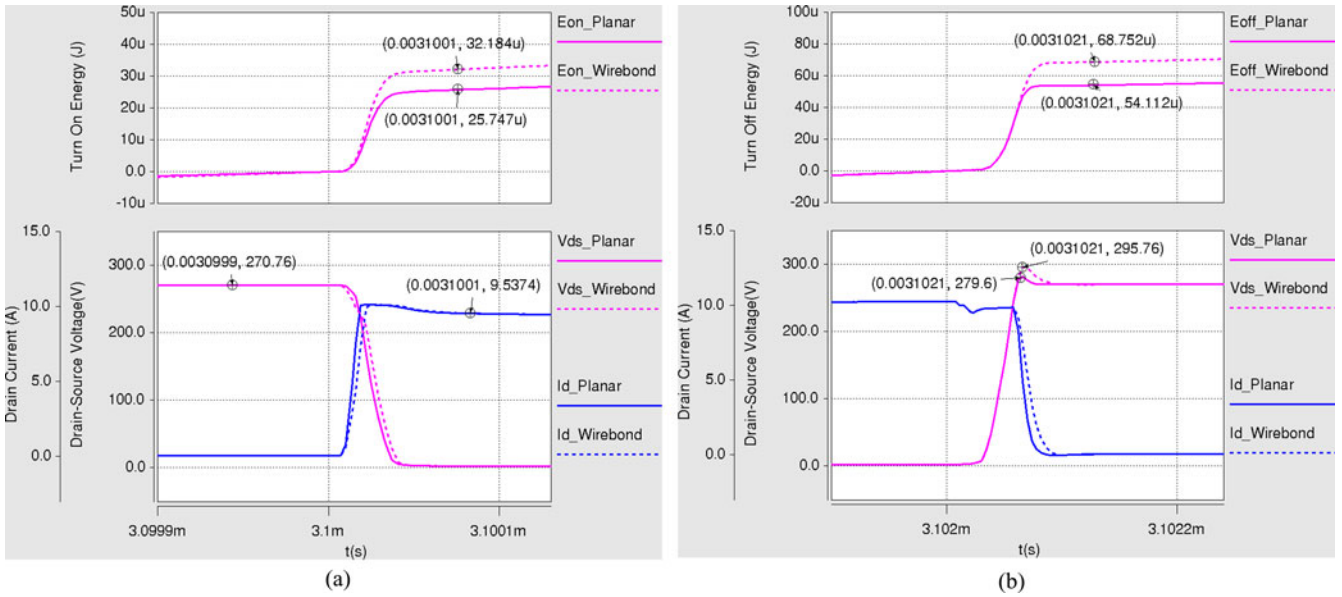
Fig. 9. Switching waveforms with different parasitics. (a) Turn-off waveforms comparison. (b) Turn-on waveforms comparison.
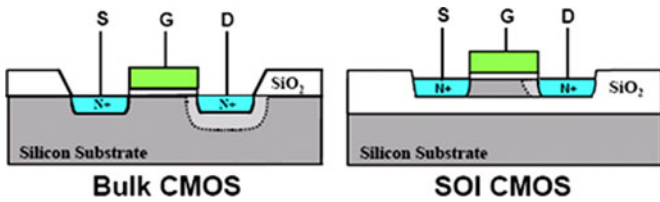

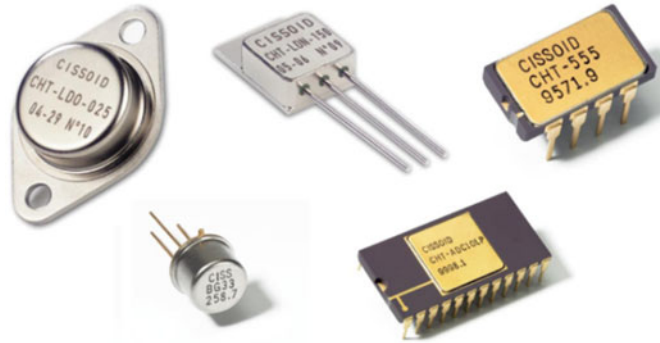Fig. 10. Structure comparison between bulk CMOS and SOI CMOS.

Fig. 11. HT SOI components from Cissoid.

Fig. 12. Summarized HT capacitors.

B. Isolated Gate Drive Design

A gate drive circuit usually provides a connection between a low-power signal IC and the system power devices. Theoretically, both optical and magnetic components can transfer the signal and power from the signal IC to the power device [27]. However, since there are no commercial HT optocouplers available, transformer isolation becomes a good choice for HT-isolated gate drive implementation. The targets for the HT gate drive circuits can be summarized as wide duty cycle range, statically turn on or off, fast speed, smaller core, and simple topology. Because of the wide duty cycle range and smaller core requirements, only the pulse transformer gate drive solutions are
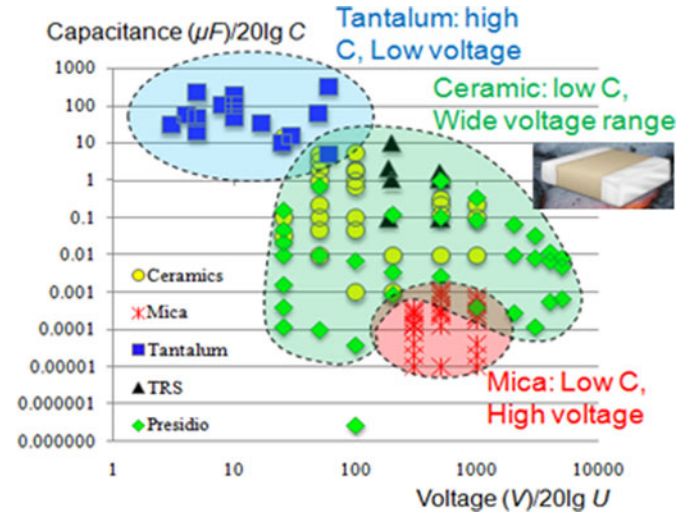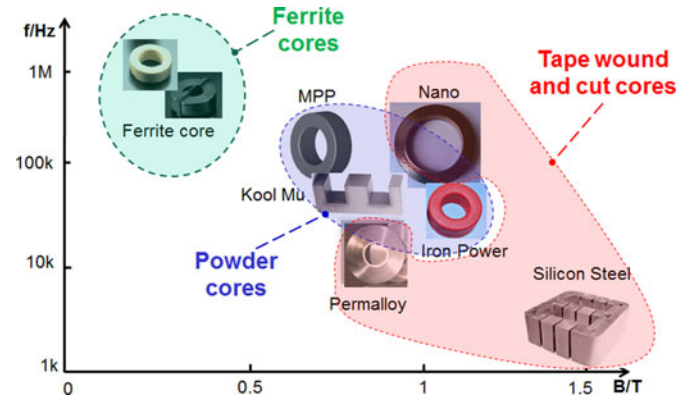

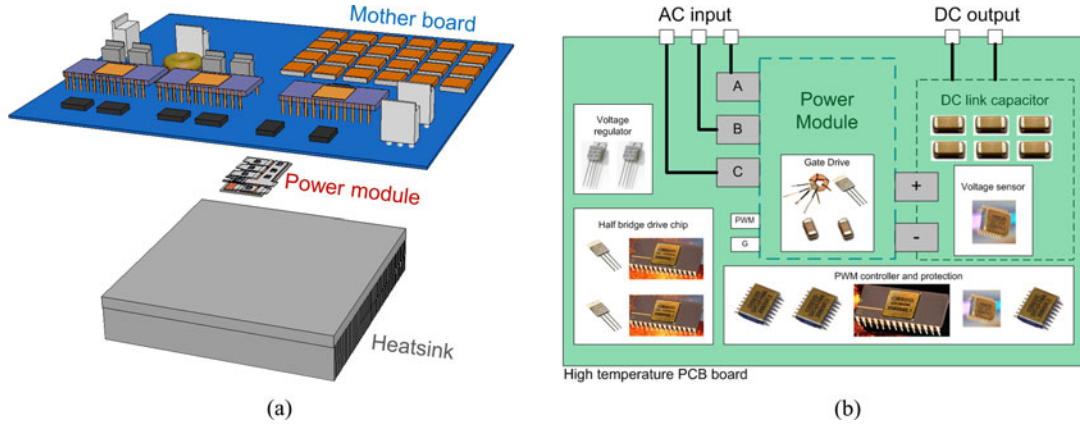Fig. 13. Summarized HT magnetic components.

Fig. 14. System structure and motherboard functions definition. (a) System structure. (b) Motherboard functions definition.
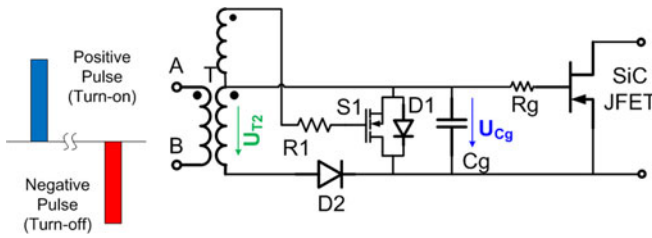

Fig. 15. Edge-triggered gate drive circuit.

Fig. 16. Turning ON and turning OFF the JFET. (a) Positive pulse to turn ON the JFET. (b) Negative pulse to turn OFF the JFET.

considered. Both the high-frequency modulation method and the edge-triggered method can be utilized. After a literature survey and a comparison of different transformer-isolated gate drive circuits [6], [25], [28], [29], one edge-triggered gate drive circuit is selected for this application because of its better thermal performance, faster speed, and simple topology. Its schematic is shown in Fig. 15.

The topology is composed of a three-terminal transformer, secondary MOSFET S1, secondary diode $D2$, and gate capacitor Cg. The body diode of the MOSFET is depicted as $D1$. Since this topology is a pulse transformer-isolated gate drive, the positive pulse or negative pulse are applied to the primary side of the gate drive to turn ON or turn OFF the SiC JFET. When the positive pulse is applied on the primary side, the secondary-side MOSFET S1 is turned ON, which shorts the gate capacitor Cg to turn ON the JFET. When the negative pulse is applied on the primary side, the gate capacitor is charged to the negative voltage through diode $D2$, and the negative voltage needs to be lower than the gate threshold value to turn OFF the JFET. After the negative pulse, the negative voltage can be held in the gate capacitor, and continue to turn OFF the JFET until another positive pulse is applied to turn ON the JFET. The two subintervals are shown in Fig. 16. For this edge-triggered gate drive circuit, both the signal and power are transferred from the primary side to the secondary side within the pulses. Since there is leakage current in the secondary gate drive circuit from both switch S1 and the JFET gate-to-source channel, the gate charge of capacitor Cg will decrease during the turn-off interval. A refreshing function needs to be applied to the primary side if the
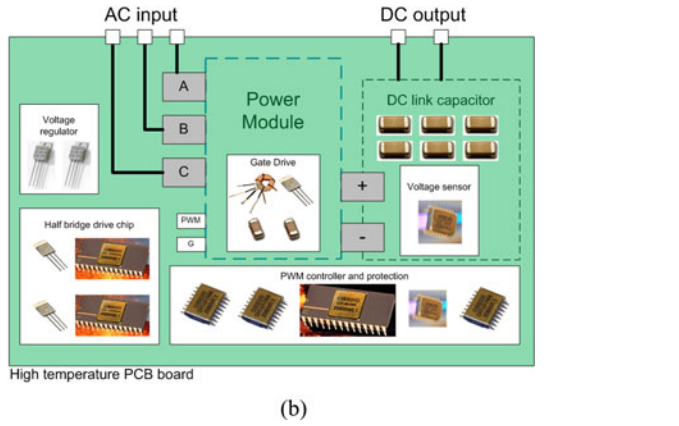
JFET needs to be statically turned OFF. For this version of the transformer, gate drive fail protection is not considered.

Because the two subinterval circuits utilize different routes for charging and discharging, the proposed gate drive can achieve independent control for both turn-on and turn-off speeds. No current-limiting resistor is required.

An 80 V voltage rating SOI HT power MOSFET (CHT-NMOS8010) from Cissoid is used for switch S1, and a 600 V voltage rating SiC diode (C3D06060A) from Cree is used for diode $D2$. This proposed gate drive topology can also be expanded to phase leg without too much modification [30].

The primary-side pulse generation function is achieved using Cissoid HT half-bridge drive chips (CHT-HYPERION).

C. Sensor and Protection Design

A dc-link voltage sensor is required for both control and protection. A nonisolated three-op-amp instrumentation amplifier structure is selected as the voltage sensor, as shown in Fig. 17. An HT quad op-amp (CMT-OPA-PSOIC16) from Cissoid is used.

It is worthwhile to note that the HT op-amp usually has a very low slew rate (1–2 V/μs) [31], which might prohibit its use in high-frequency voltage-sensing applications.

Either a thermistor or thermocouple can be used for the temperature sensor. However, the thermistor usually covers a temperature range of less than $150\,°C$, which is not suitable for HT applications. Thus, a thermocouple is used in this system. The Type T thermocouple's temperature range is from $-200\,°C$ to $350\,°C$ and has a sensitivity of about 43 μV/$°C$. The tested point of the thermocouple is embedded in the power module, and the other end of the thermocouple is connected to the motherboard, as shown in Fig. 18. The Seebeck voltage sensed by
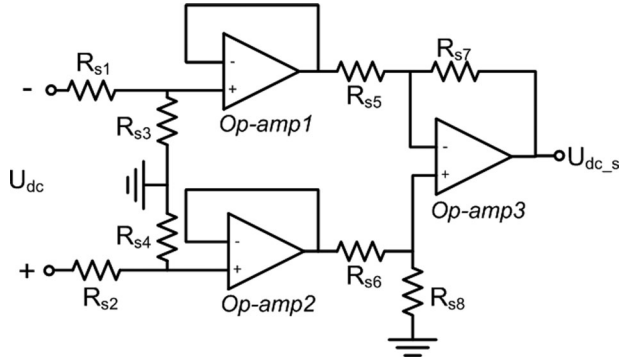
Fig. 17.   Voltage sensor topology.
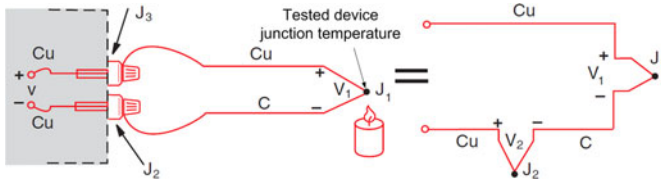

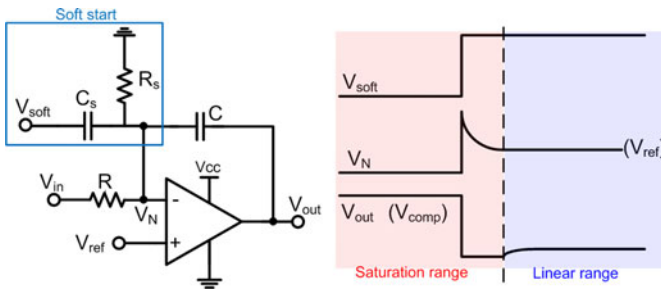Fig. 18.   Thermocouple connection in the system.

Fig. 19.   Controller and soft start.

the thermocouple is shown as follows:

$$V = \alpha[(T_{J1} + 273.15) - (T_{J2} + 273.15)] = \alpha(T_{J1} - T_{J2}).$$
(1)

Since the Seebeck voltage is very small, an amplification circuit using the HT op-amp is built in the motherboard.

Both the sensed voltage and sensed temperature are sent to the protection circuit, which is composed of HT op-amps and an HT D-type flip-flop. Once the protection is activated, the turn-on pulses will be cutoff, and only turn-off pulses are applied for the refreshing functions to statically turn OFF the SiC JFET.

D. Controller Design

An HT analog PWM controller from Cissoid (CHT-MAGMA) is used as our system controller. The controller is an analog controller, and an integral controller with a soft-start circuit is built to achieve voltage loop control. As shown in Fig. 19, the soft-start function will guarantee that the compensation voltage starts at zero, which means the duty cycle will also start at zero.

The system start process is simulated and shown in Fig. 20. This start process can be divided into two subintervals. At the
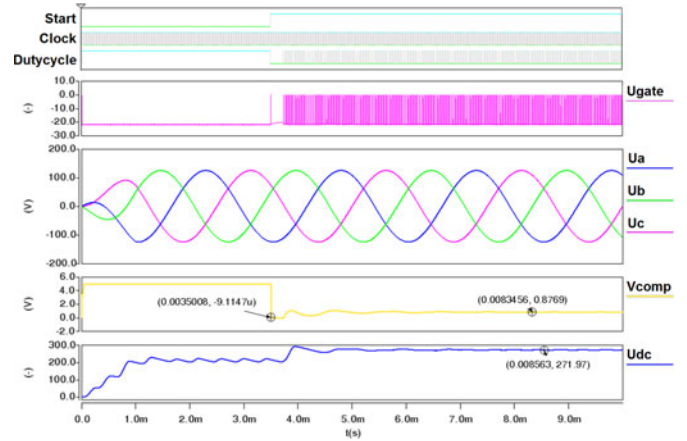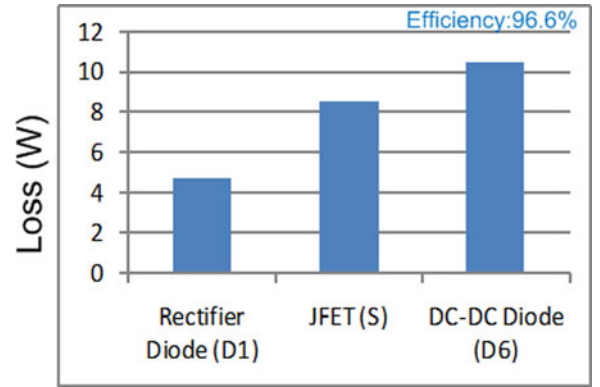

Fig. 20.   Simulation for the start process.

Fig. 21.   Loss distribution in the power module.

beginning, the JFET is always turned OFF by applying the refreshing signals that will generate refreshing turn-off pulses to the gate drive circuit. The system works as a diode rectifier. When the start signal becomes active, the system converts from diode rectifier mode to PWM rectifier mode. The dc-link voltage is regulated at 270 V. The soft-start function will gradually increase the duty cycle from zero to the rated value.

E. System Thermal Design

The targets for the system thermal design before the real test are temperature prediction and better thermal management. Once the main devices, switching frequency, and operation point are fixed, the detailed power module loss can be calculated using Saber tools. With the loss calculation results, thermal simulation tools such as IDEAS can be used to predict the temperature distribution for the power module with an assumed air-cooling speed and system layout.

In order to have a 1.4 kW power output and not exceed the peak current, which is 10 A for this device, the power module will only operate in continuous current mode (CCM). The loss distribution for different components based on the CCM mode of operation is summarized in Fig. 21.

The thermal performance simulation results with detailed loss distribution for the power module are shown in Fig. 22, and were
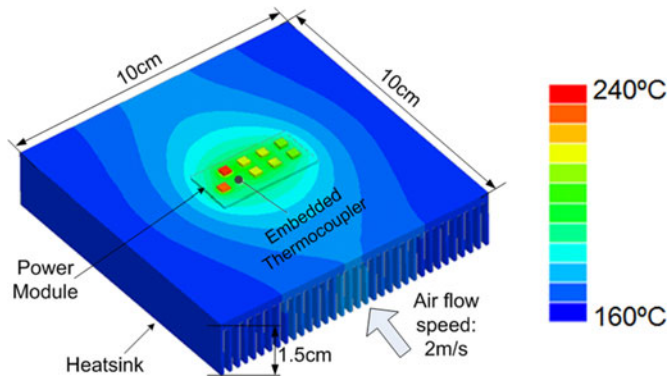
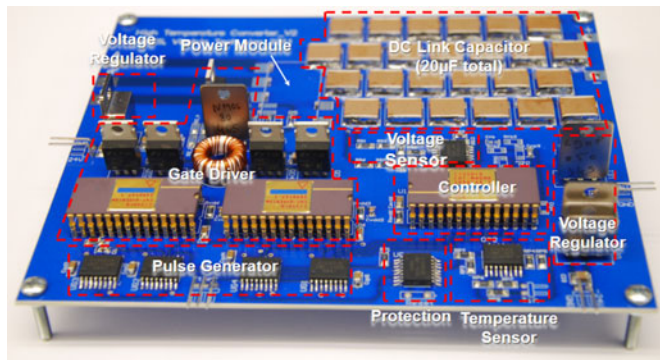Fig. 22. Thermal performance simulation results for the power module.

Fig. 23. System prototype.

created with the simulation tool IDEAS. Computational fluid dynamics, thermal coupling, and open air-to-ambient boundary conditions are adopted. With the assumption of 100 °C ambient temperature, heatsink dimensions of 10 × cm 10 cm × 1.5 cm, and 2 m/s airflow speed, the maximum junction temperature of the power module reaches 240 °C, which is lower than the designed maximum value of the planar structure power module. The embedded thermocouple position is marked in the figure.

The 1.4 kW system prototype is shown in Fig. 23. All the functions are defined and marked in the figure. The dimensions of the motherboard are 16.5 cm × 14 cm, and the planar structure power module is put under the motherboard, as indicated in the figure. The figure also shows that the power module occupies only a small portion of the footprint of the converter. The section in the following contains a detailed discussion about power density and benefits of HT converter design.

V. EXPERIMENTAL RESULTS

To verify the unit's ability to operate in a harsh environment, both the components and the system are tested and debugged. This section shows the results of thermal tests on some HT components and the HT converter debugging process in a harsh environment condition emulated by thermal chamber.

A. Components Thermal Test

As shown in the surveyed HT capacitor results in Fig. 12, ceramic capacitors are selected for both the dc-link capaci-

tors and the control capacitors. Because surface-mounted chip capacitors are susceptible to fracture from thermally induced stresses, which may be caused by the capacitor itself or by the soldering process [32], the larger volume or thicker ceramic capacitors such as the dc-link capacitors (500 V, 0.4 μF, 3941XHT404M6P5) may make the thermal stress problem more severe.

The MIL-STD-883H standard [33] was used as a reference to conduct the thermal-cycling tests for evaluating the reliability of the HT ceramic capacitors under thermal stress. Meanwhile, the HT PCB board (Roger 4350) and HT solder are also verified using the thermal-cycling test.

A Tenney TUJR thermal-cycling chamber is used for testing. Fig. 24 shows the thermal-cycling chamber and profile. The thermal-cycling temperature ranges from −50 °C to 200 °C. Each cycle lasts for 1 h, and the hot and cold temperature duration time is 13 min. The maximum slope that we can achieve is roughly 20 °C/min.

For the ceramic capacitor, the middle electrode layers usually have a higher CTE than the ceramic layer, which tends to force the capacitor apart when heated. In addition, after the ceramic capacitors are soldered to the HT PCB, the PCB and solder CTE may also increase the thermal stress at the terminal and cause the capacitors to crack. To verify the thermal reliability of the HT capacitors, ten pieces of HT dc-link ceramic capacitors' samples were divided into two groups: five bare capacitors comprised Group 1, and five capacitors soldered on top of the HT PCB board (Roger 4350) comprised Group 2. Different solder shapes were employed for Group 2. All these samples are put into the thermal-cycling chamber for cycling.

After the thermal cycles, the samples were mounted in molding epoxy for cross sectioning and polishing. The cross-sectional view of these tested samples under microscope (STEMI-2000-C) is shown in Fig. 25. Fig. 25(a)–(c) indicates the samples that were soldered on the HT PCB board with large, medium, and small solder shapes. Fig. 25(d) illustrates the bare capacitors without soldering on top of the PCB board in Group 1. The bare capacitor has no crack observed even after 600 cycles. As shown in Fig. 25(a), a larger solder shape will generate more thermal stress to the capacitor and can create cracks even after only 150 cycles. Reducing the solder shape will help to reduce the thermal stress seen in Fig. 25(b) and (c). After 300 thermal cycles, the Group 2 samples with a small solder shape have no obvious changes in terms of appearance, capacitance value, or breakdown voltage level. In order to use the ceramic capacitor in HT applications, we need to control the solder shape to a small value. To further reduce thermal stress and improve the ceramic capacitor thermal reliability, external through-hole leads can be utilized. Meanwhile, no obvious change is observed after 300 thermal cycles for the HT PCB and solder.

Besides the HT capacitor thermal reliability test, the HT low-permeability NiZn ferrite toroid cores (4C65) from Ferroxcube are also tested with respect to different ambient temperatures using the core loss measurement method shown in [34]. Fig. 26 shows the HT ferrite core loss measurement setup and results. The small HT core used for the gate drive is dipped into the HT heat transfer oil, whose temperature is controlled by the hotplate.
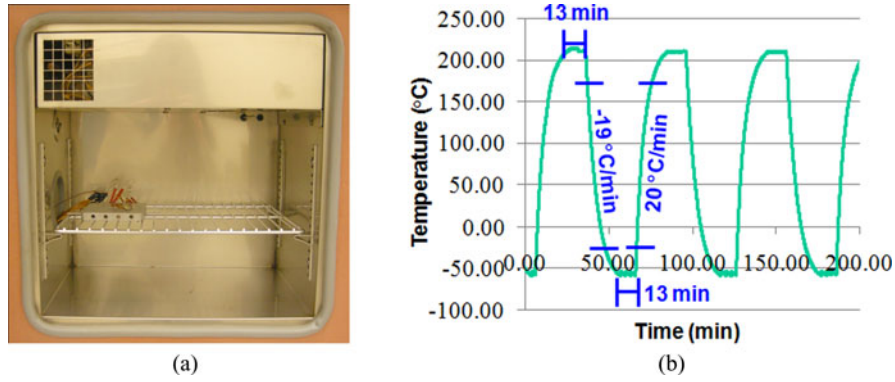
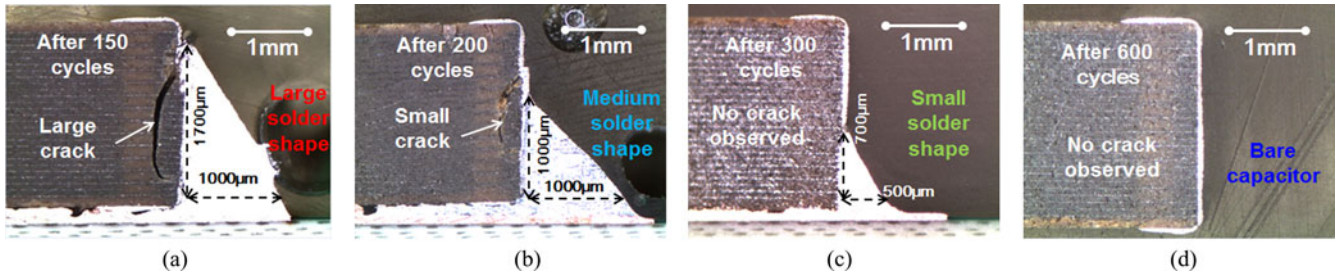Fig. 24. Thermal-cycling chamber and profile. (a) Tenney environment chamber. (b) Tested temperature profile.

Fig. 25. Thermal-cycling test for the HT ceramic capacitor and cross-sectional view (-55–$200\,°C$). (a) Large solder shape in Group 2. (b) Medium solder shape in Group 2. (c) Small solder shape in Group 2. (d) Bare capacitor in Group 1.
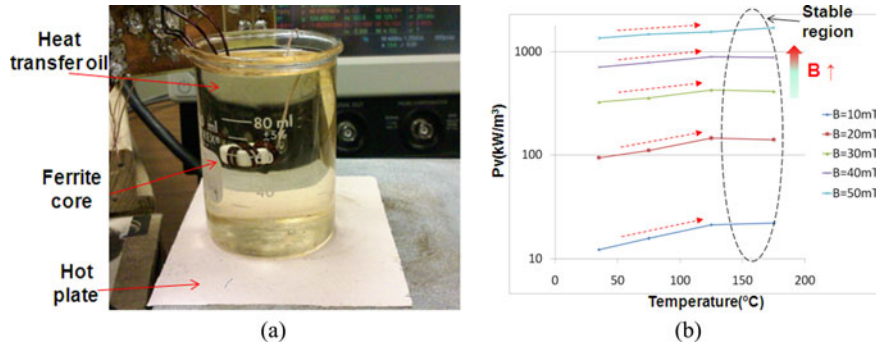

Fig. 26. HT ferrite core loss measurement. (a) Core loss measurement setup. (b) Core loss measurement results.

Several different excitation frequencies are used to measure the core loss. Fig. 26(b) shows the core loss measurement results for one exciting frequency point (1 MHz). For most saturation flux values lower than 50 mT, the HT ferrite core loss will increase when the temperature increases from room temperature to $125\,°C$ ambient. After that, the core loss will stabilize, which guarantees that this inductor will not have the thermal runaway problem. For the real design, the primary-side number of turns is selected to be 9, so the maximum flux density will be controlled to a value less than 40 mT, as shown in (2). Since the tested stray capacitance between the transformers on the primary side and the secondary side is less than 6 pF, the designed gate drive circuit will not suffer the *dv/dt* immunity issue

$$B_{\max} \le \frac{u \cdot t_p}{n_1 \cdot A_c} = 40 \text{ mT}. \qquad (2)$$

B. System Harsh Environment Test

With consideration of the thermal chamber inner space, the Envirotronics thermal chamber is selected to emulate the harsh environment for the soaking test. Nine different ambient temperature test points with $25\,°C$ steps from $-50\,°C$ to $150\,°C$ were tested.

Fig. 27 shows the converter inside the thermal chamber. The thermal chamber creates a harsh environment, with temperatures ranging from $-50\,°C$ to $150\,°C$. The thermocouple, $200\,°C$ monitor wires, and power wires are connected outside the chamber through a hole that is sealed with a sponge plug. Several key point temperatures monitored by the thermocouple are marked in the figure. Due to a lack of HT fans that we can put inside the thermal chamber, the motherboard test and the power test are conducted separately inside and outside the thermal chamber.
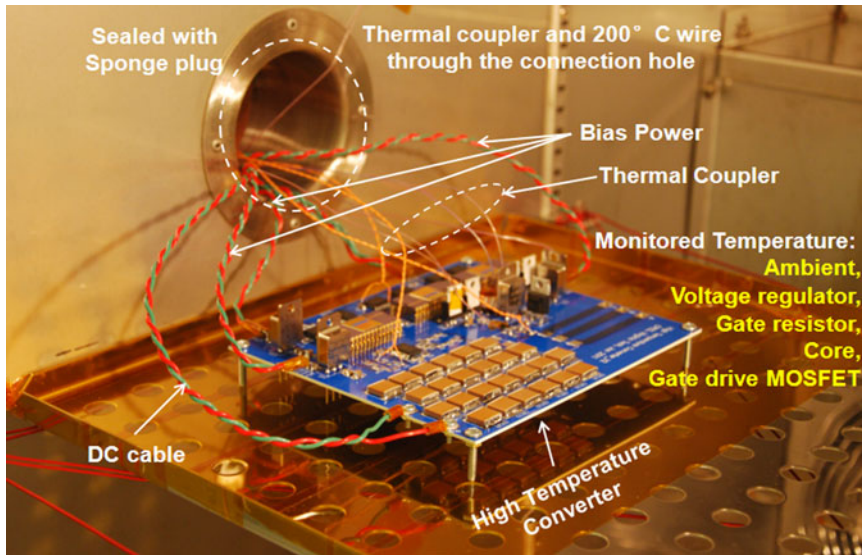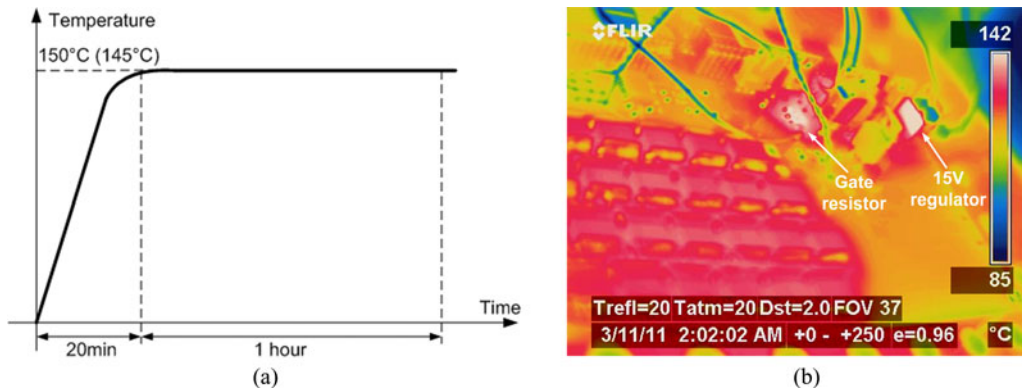
Fig. 27. Converter inside the thermal chamber.

Fig. 28. Temperature profile and thermal camera picture after 150 $^\circ$C soaking test. (a) Temperature profile for the soaking test. (b) Thermal camera picture after the soaking test.

For the motherboard test inside the chamber, the system is working as an open loop, and the fixed duty cycle is set. All the functions except the power module can be verified during the nine temperature soaking tests. The 150 $^\circ$C ambient temperature soaking test is shown in Figs. 28–30. Fig. 28(a) shows the temperature profile for the 150 $^\circ$C soaking test. The temperature inside the thermal chamber increases from room temperature to 145 $^\circ$C (the steady state is 5 $^\circ$C less than the reference, as monitored by the thermocouple) within 20 min. Then, the thermal chamber temperature stays constant for 1 h. Fig. 28(b) shows the thermal camera picture after the 150 $^\circ$C soaking test. After the soaking test, the thermal chamber door is opened, and a picture is taken with the thermal camera outside the chamber. Because of the long distance between the thermal camera and the HT converter, the value shown in the thermal picture may have some error. In addition, the internal metal case of the thermal chamber also reflects some infrared due to the ambient temperature after we open the door. However, we can still clearly see that the gate resistor and 24–15 V voltage regulator are the hottest spots.

The PWM generation by the controller is shown in Fig. 29. The HT CHT-MAGMA PWM controller is selected as our con-

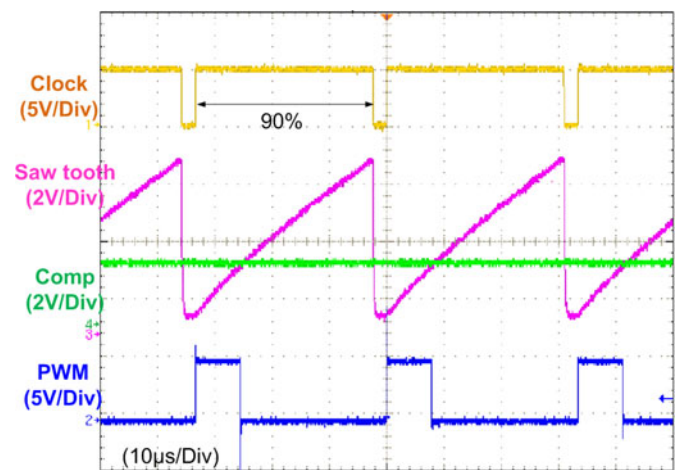Fig. 29. PWM generator test in 150 $^\circ$C soaking environment.

troller in the system. A constant 30-kHz clock signal is generated by the internal oscillator circuit together with the outside *RC* components. The clock signal duty cycle is 90%. During
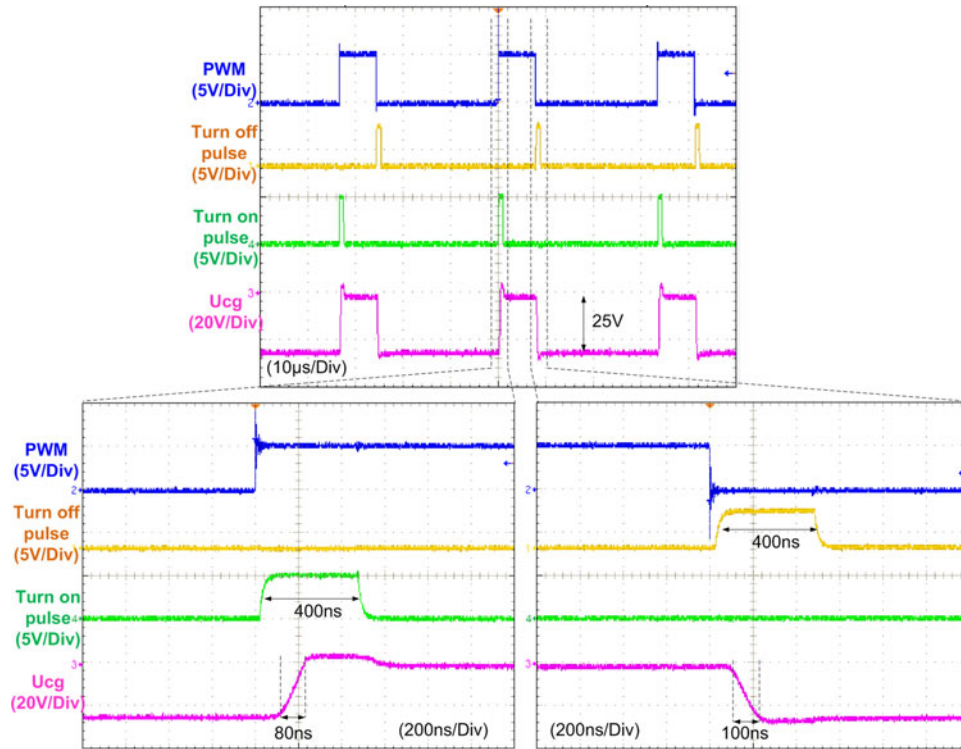
Fig. 30.   Edge-triggered gate drive circuit test results in 150 °C soaking environment.
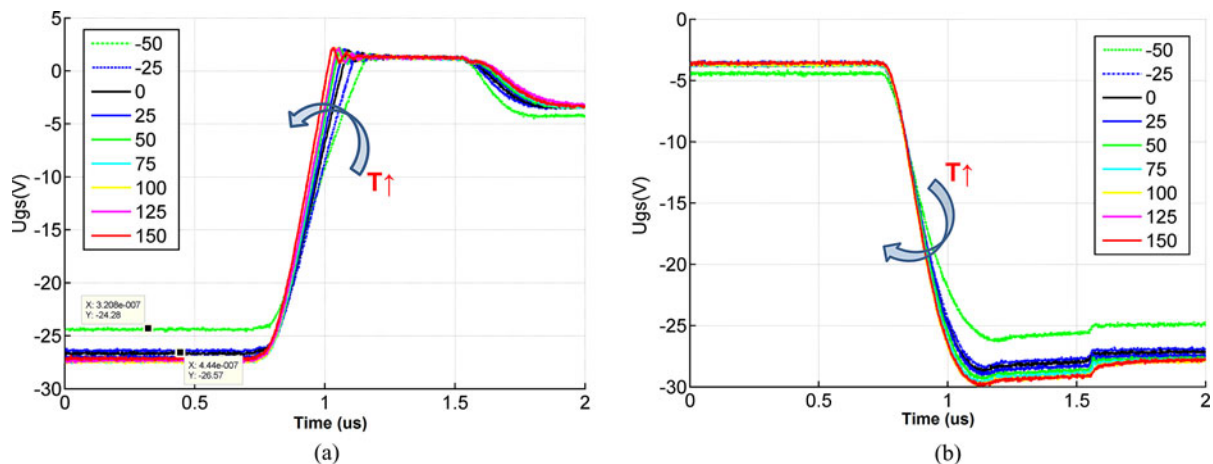

Fig. 31.   Monitored gate drive signal during harsh conditions. (a) Turn-on slope. (b) Turn-off slope.

the high logic of the clock signal, the sawtooth signal is linearly charged to its maximum value. The sawtooth signal is clamped at zero when the clock signal is at a low level, which means the maximum duty cycle generated by the controller will not exceed 90%.

Fig. 30 shows the test results of the proposed edge-triggered gate drive circuit. The tested stray capacitance between the transformer primary side and secondary side is less than 5 pF. The PWM signal coming from the PWM controller is sent to the pulse generation circuit, which will generate both turn-on and turn-off pulses. The width of the pulse is 400 ns. When a positive pulse is applied on the primary side, the secondary-side MOSFET is turned ON, which will also turn ON the JFET. The

turn-on gate slope is 80 ns. When a negative pulse is applied on the primary side, the gate capacitor is charged to the negative voltage (−25 V) through diode $D2$, which will turn OFF the JFET. The turn-off gate slope is 100 ns.

The influence of different ambient temperatures on the converter performance is demonstrated in Figs. 31–34. Fig. 31 shows the monitored gate drive signal in different harsh environments. Both the turn-on and turn-off slopes become faster when the ambient temperature increases. The major reason for this is because the value of X7R capacitor Cg (4 nF) from Fig. 15 will decrease 20% when the temperature goes up to 150 °C. Besides the gate drive speed, the steady-state turn-off gate drive voltage is also influenced by different ambient
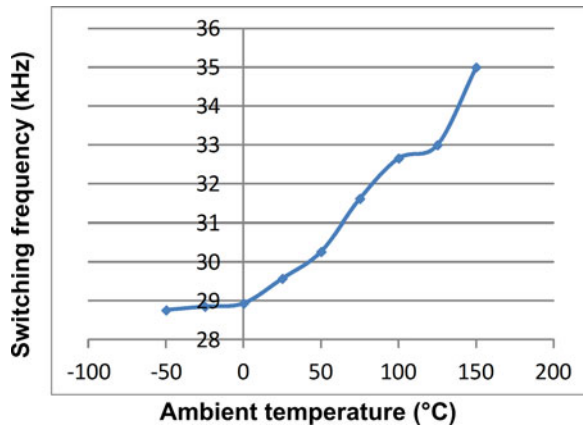
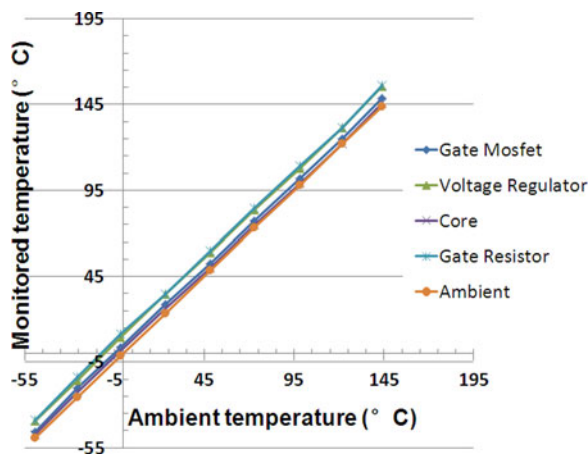Fig. 32. Monitored switching frequency during harsh environment.

Fig. 33. Monitored temperature point.

temperatures. When the ambient temperature goes to −50 °C, the voltage is −24.3 V. This is because the output voltage of the 15 V voltage regulator (CHT-LDOP-150) will decrease when the ambient temperature decreases, especially when the ambient temperature reaches −50 °C. Since the primary-side supply voltage decrease will lead to a voltage drop on the secondary side, the pulse transformer gate drive circuit will be sensitive to the supply voltage on the primary side.

Fig. 32 illustrates the monitored switching frequency with different harsh environments. As mentioned previously, the switching frequency signal is generated by the clock output pin of the HT analog controller chip (CHT-Magma), as shown in Fig. 29. The clock signal is generated by an internal oscillator with both internal and external *RC* components. The passive components temperature dependence will cause a 15% change of switching frequency when the temperature increases from −50 °C to 150 °C.

The monitored temperatures for all the test points are summarized in Fig. 33. As shown in Fig. 28(b), the gate resistor and voltage regulator are the hottest spots in the system. All other monitored temperatures are within 10 °C above the ambient temperature.

Since the controlled dc-link voltage is 270 V, the voltage sensor conversion ratio is designed to be 100. Fig. 34 shows the voltage sensor test at different ambient temperatures. Because of the three-op-amp structure shown in Fig. 17, the input resistor's positive temperature coefficient will be canceled, and the voltage sensor results stay almost the same for different ambient temperatures. The voltage variance for different testing points can be controlled to be less than 30 μV.

The power test with both the motherboard and power module is conducted outside the thermal chamber, since no HT fans are available that we can put into the thermal chamber. The power test was conducted with only natural cooling outside the thermal chamber without fans. The test waveforms are shown in Fig. 35. The planar structure power module operated stably with 100 V input voltage (phase to neutral), 400 Hz supply frequency, and 5 A output current. Besides the embedded thermocouple that closes to the SiC JFET, another thermocouple is utilized to measure the heatsink temperature. The distributed temperatures during the power test and tested efficiency are shown in Table IV. After 30 min, the module temperature reaches the steady state. The junction temperature is 227 °C, which is measured with the embedded thermocouple. A temperature difference of around 20 °C is estimated between the embedded test point and the real junction based on the thermal simulation in Fig. 22. The converter total efficiency is 96.5% for a 250 °C junction temperature, which is 0.8% lower than at room temperature. The test results prove that the developed planar package SiC power module can support operation at a 250 °C junction temperature.

Die-attachment thermal reliability is a common concern for power modules. Since the nanosilver paste is selected as the die-attachment material, the nanosilver paste thermal reliability performance is critical to the whole module. Although no destructive test is directly applied to the planar structure power module, previous studies [35]–[37] already demonstrate that nanosilver paste has good thermal reliability performance with respect to both the thermal-cycling test and the thermal soaking test. Meanwhile, substrate thermal reliability is also a bottleneck for the HT converter. By utilizing a sealed step edge for the copper [10], the peeling stress in the edge and corner of the substrate can be relieved. In addition to these tests, more thermal reliability tests will be conducted with respect to different layers interconnection in the planar structure power module.

VI. DISCUSSION

A. Test Results Discussion

Based on the test results, the HT power module in a planar structure meets the requirement of 250 °C junction temperature. Compared with a traditional wire bonding packaging structure, the planar packaging structure will have a smaller footprint and smaller parasitics, which will lead to less loss and voltage stress to the devices. Therefore, the planar packaging structure is more suitable for SiC HT applications. In addition to this, the 3-D lead frame structure of the planar power module will provide more flexible routing. However, pushing the device junction temperature to a higher value will increase the system loss and decrease the efficiency, as shown in Table IV. The major reason
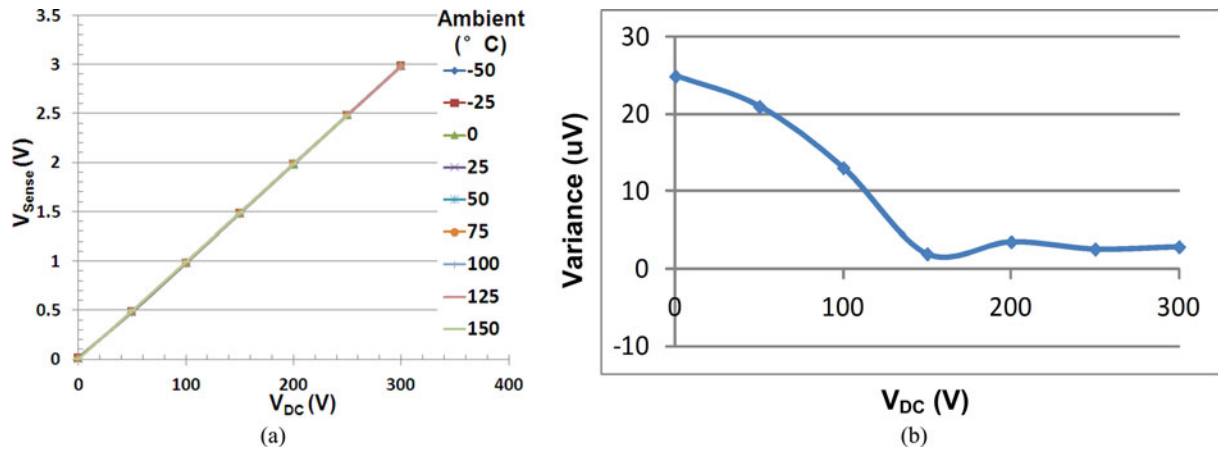
Fig. 34.   Voltage sensor test in harsh environments. (a) Voltage sensor test results. (b) Voltage sensor variance results.
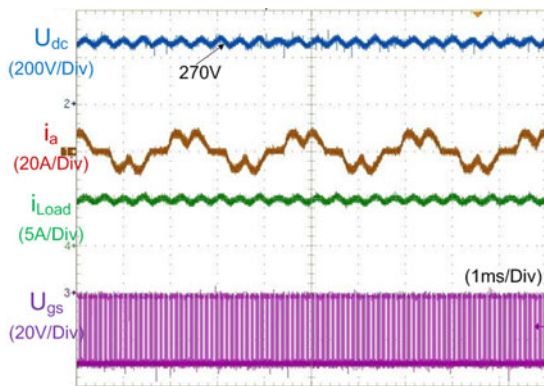

Fig. 35.   Continuous power test results (1.4 kW, 250 °C junction temperature).

TABLE IV
MEASURED TEMPERATURE DISTRIBUTION AND EFFICIENCY

Time	JFET	Heatsink	Efficiency
0:00 minutes	24.5°C	24.5°C	97.3%
30:00 minutes	227°C	128°C	96.5%
40:00 minutes	227°C	129°C	96.5%

for the higher loss is due to the positive temperature on resistance of the SiC diode and JFET as indicated in Fig. 6.

Besides the power module, the motherboard provides the capability of working up to 150 °C ambient temperature. In order to achieve this, SOI chips together with other HT components are utilized to provide the functions as sensor, protection, controller, gate drive, and filter. The proposed edge-triggered gate drive method is verified in HT applications with simple topology and smaller loss. The hotspot of the gate resistor is only 12 °C higher than the ambient temperature. However, since both the power and signal are transferred from the gate drive primary side to the secondary side within the pulses, refreshing functions need

to be designed to statically turn OFF the JFET. Meanwhile, the gate drive speed and turn-off voltage level will be influenced by the passive components and voltage regulator temperature characteristics. An HT analog controller is utilized in this prototype, and the switching frequency may change due to the passive components' temperature dependence. Three-op-amp structure voltage sensors cancel the temperature dependence effect of the passive components, and are suitable for HT applications. An HT ceramic capacitor is adopted to achieve the dc-link filtering function. In order to increase the thermal reliability of the ceramic capacitor, thermal stress needs to be reduced by using a smaller solder shape or an external through-hole lead frame.

B. Power Density Discussion

As mentioned previously, the fabricated HT system is not as compact as we expected. The total weight of the 1.4 kW HT prototype is 277 g, and the detailed weight distribution picture is shown in Fig. 36(a). Actually, the fabricated prototype is heavier than the equivalent low-temperature converter with a similar power level, as shown in Fig. 36(b). For the HT version converter, the PCB board and the related control electronics compose a large share of more than 45% of the total weight. This is because of the larger footprint and heavier weight for the HT components, such as SOI or a complicated transformer gate drive design, due to the limited choice of available components. However, this weight ratio may decrease when the converter power level increases. Then, the heaviest parts will be the power module, heatsink, and filter. However, if we compare the weight between the HT version and low-temperature version, the heatsink and power module may not be too different, because there is a similar temperature difference between the junction and ambient. However, because of the high ambient temperature, the HT ceramic capacitor is much heavier than the low-temperature version, which still makes the HT converter heavier than the low-temperature converter.

However, an HT converter will bring system-level benefits. The potential applications of an HT converter can be transportation applications, such as vehicles, aviation, and marine applications. Adoption of more electrical systems in modern
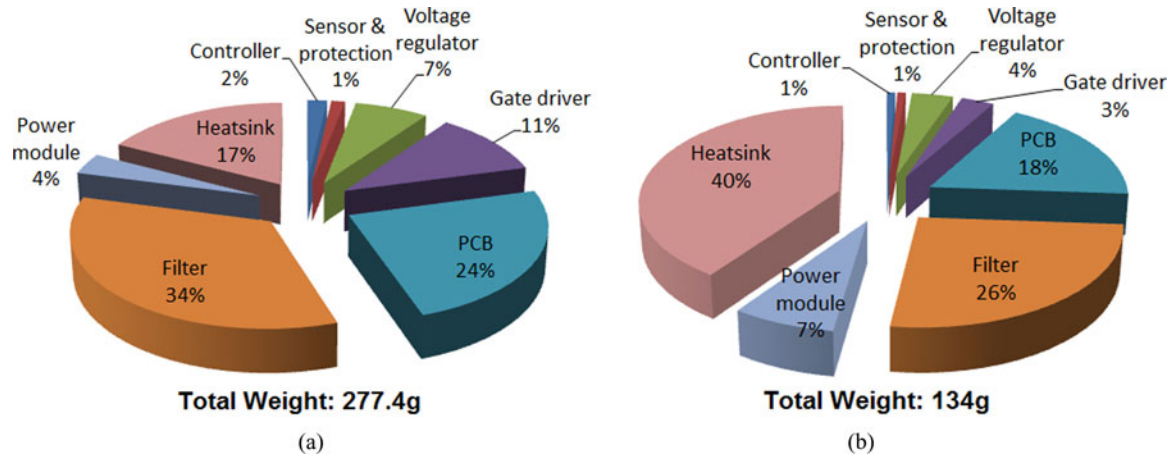
Fig. 36. Weight distribution of the 1.4 kW converter prototypes. (a). HT version (150 °C ambient temperature, 250 °C junction temperature) (b). Low-temperature version (25 °C ambient temperature, 125 °C junction temperature).

transportation will bring benefits to the whole system by reducing the complexity, and can replace traditional mechanical, pneumatic, or hydraulic power. In addition, the total system weight will be reduced and the system power density will be increased, which will reduce fuel consumption while simultaneously reducing emissions. Thus, to design an electrical converter that can work in harsh environments is both critical and valuable. Besides transportation applications, deep-earth petroleum exploration applications also require electrical converters that can work in harsh environments.

Generally speaking, the HT converter design is possible, but still constrained by available components. With current technology, HT converters will have a higher cost, heavier weight, and larger volume than equivalent low-temperature converters. Besides the semiconductor devices and related HT packaging methods, the development of auxiliary components, such as HT control electronics and HT passive components, is desired.

VII. CONCLUSION

This paper presents the detailed design process of an HT SiC three-phase ac–dc converter. SiC diodes and JFETs are used as the main circuit devices, and are packaged in a novel HT planar structure that can support a 250 °C junction temperature. An edge-triggered HT gate drive solution is also proposed to drive the designed power module. In addition, all system functions, such as the controller, regulator, filter, sensor, and protection, are integrated into the HT system based on HT passive SOI chips and auxiliary components. The tests on the prototype in harsh environments prove the feasibility of HT operation up to 150 °C. The system performance with different ambient temperatures is also analyzed.

Further work could be conducted in this area. First, since the planar structure utilizes 3-D lead frames, more thermal reliability studies related to layered interconnection need to be explored. Moreover, HT EMI filter design could also be a topic for the future work.

APPENDIX

TABLE V
SURVEY OF HT RESISTORS

Material	Vendor	Temperature
Carbon film	KOA Speer Electronics	-55 ~ 200 °C
Ceramic	Ohmite	-40 ~ 220 °C
	KOA Speer Electronics	-40 ~ 200 °C
Metal stripe	Vishay	-65 ~ 275 °C
Metal film	KOA Speer Electronics	-55 ~ 200 °C
	Vishay	-65 ~ 225 °C
Metal Oxide	IRC	-55 ~ 200 °C
Flip chip film	Ohmite	-55 ~ 200 °C
Wirewound	Bourns	-55 ~ 275 °C
	Vishay	-65 ~ 275 °C
Thick film	IRC	-55 ~ 200 °C
	Ohmite	-55 ~ 200 °C

TABLE VI
SURVEY OF HT CAPACITORS

Materials		Vendor	Capacitance	Temperature
Ceramic	NP0	Kemet Novacap	1.0pF~ 0.12μF	-55~200°C
	X7R	Johanson Dielectric Eurofarad	100pF~ 3.3μF	-55~200°C
Teflon		Eurofarad	470pF~2.2 μ F	-55~200°C
Tantalum		Kemet	0.15μF~ 150μF	-55~175°C
Mica		CDE	1.0pF~1500pF	200°C

TABLE VII
SURVEY OF HT MAGNETICS

Vendor	Series	Inductance range	Temperature range
Vashay	TJ3-HT	0.39 ~ 100 μH	-55 ~ 200 °C
	TJ5-HT	0.47 ~ 470 μH	-55 ~ 200 °C
Datatronic	Dr-360	1.2 ~ 1000 μH	-55 ~ 200 °C
	Dr-361	1.2 ~ 1000 μH	-55 ~ 200 °C
	Dr-362	1.0 ~ 1000 μH	-55 ~ 200 °C
Ferroxcube	4C65		Up to 200°C
	3C93		Up to 200°C

ACKNOWLEDGMENT

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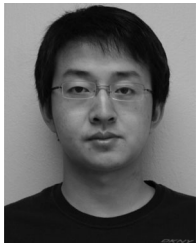
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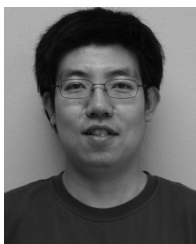
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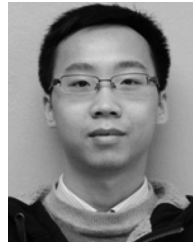
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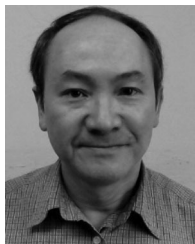
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